Low Turn-off Switching Energy 1200V IGBT Module

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Abstract - **A new 5th generation IGBT module with low turn-off energy has been developed. The module utilizes IGBT chips optimized for high frequency industrial power supplies in applications such as X-Ray, MRI (Magnetic Resonance Imaging), and induction heating. This technology is designed to provide a simplified cost effective alternative to parallel discrete MOSFETs in these applications.**

I. INTRODUCTION

Standard industrial IGBT modules are usually optimized for motor drive and similar applications in which the carrier frequency is typically 15kHz or less. For these applications conduction losses tend to dominate so the IGBT chip is optimized primarily for low $V_{CE(SAT)}$. Despite this optimization these modules have found increasing application in high power industrial applications such as medical, laser, telecommunication, induction heating, and welding power supplies. In these applications higher operating frequencies are usually desired to improve performance and reduce the size of magnetic components. At higher operating frequencies turn-off switching losses become dominant and usually severely limit the usable capability of standard modules. Newer generation modules having both lower $V_{CE(SAT)}$ and lower turn-off losses offer improved performance in high frequency applications but are still limited by their relatively high turn-off losses. Fortunately, new module packages have been developed with significantly reduced internal inductance making it possible to support faster switching IGBT chips. This paper presents a new module developed using a standard low inductance package with new IGBT chips optimized for low turn-off switching losses.

II. 5TH GENERATION IGBT CHIP – THE CSTBT

Fig. 1 shows an equivalent circuit model for an ideal IGBT in its on state. This circuit shows that the on-state voltage ($V_{CE(SAT)}$) of an IGBT can be thought of as the sum of the forward voltage of a PIN diode and the $R_{DS(ON)}$ drop of a MOSFET. The $R_{DS(ON)}$ of the MOSFET portion of Fig. 1 can be decreased by increasing the total channel width per unit chip area. High-density trench gate surface structures have been developed to provide a substantial increase in channel width [2][10][11][14]. At the same time the trench gate structure eliminates the parasitic JFET resistance associated

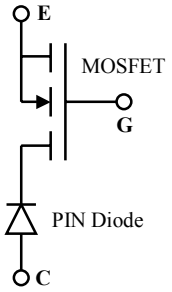

Fig. 1 On-State Model of IGBT

with the MOSFET. As a result, the largest component of on-state voltage in state-of-the-art trench gate IGBT devices can be linked to the forward voltage drop of the PIN diode portion of Fig. 1.

Normally a PIN diode has a symmetrical excess carrier distribution in the n- region as shown by curve A in Fig. 2. Curve B shows that the excess carrier distribution in a conventional trench gate IGBT deviates from the ideal case by steadily decreasing as it approaches the emitter side of the device. This non-ideal behavior becomes even more pronounced in devices with high blocking voltage ratings. The decreased carrier concentration near the emitter side effectively increases the resistance of the PIN diode which

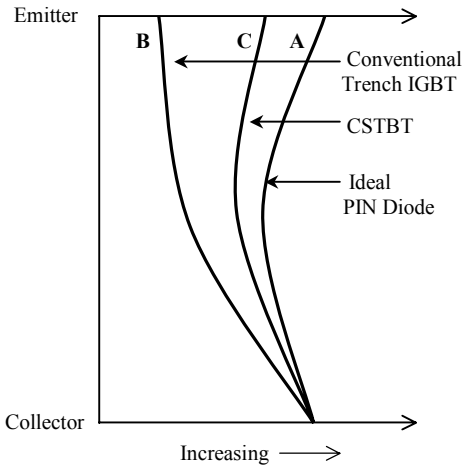

Fig. 2 Excess Carrier Distribution in the n- Layer

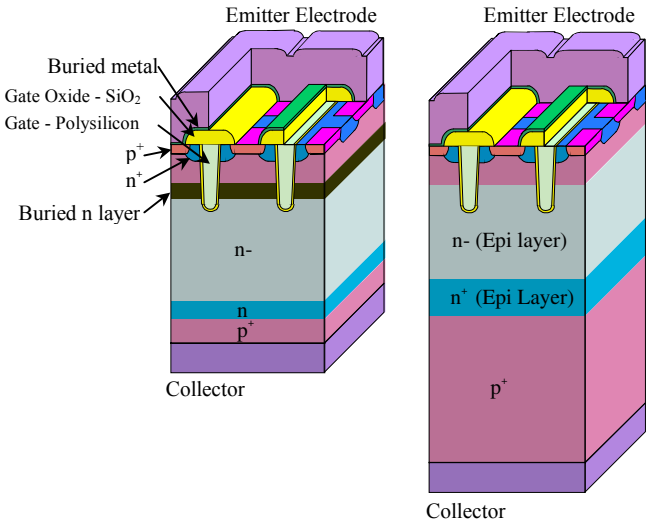

Fig. 3a New CSTBT Chip Fig. 3b Conventional Trench Gate IGBT

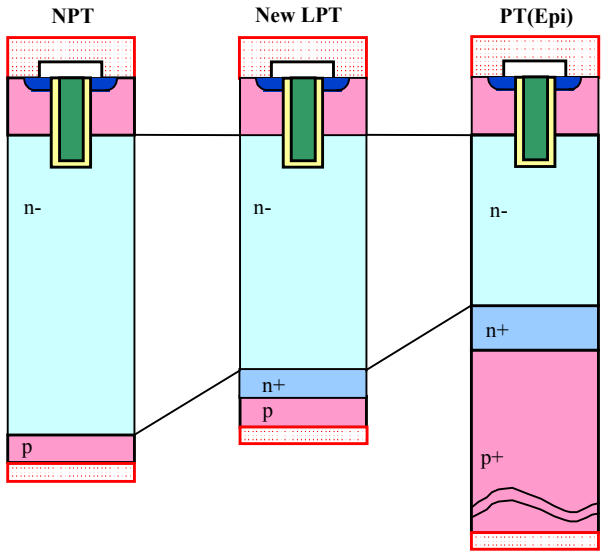

Fig. 4 Comparison of IGBT Vertical Structure

results in an increase in on-state voltage ($V_{CE(SAT)}$). To improve the carrier concentration at the emitter side a new chip design called Carrier Stored Trench Bipolar Transistor (CSTBT) has been developed. The CSTBT is fabricated with an additional n type buried layer. The buried layer provides "stored" carriers to produce the modified carrier distribution shown in curve C of Fig. 2. The resulting carrier distribution is closer to the ideal case and produces increased conductivity in the n- layer. The result is a substantial reduction in the on-state voltage of the device. Fig. 3a and 3b show the cell structure of a conventional high cell density trench gate IGBT compared to the CSTBT. The key difference is the addition of the buried n layer to provide increased carrier concentration near the emitter side of the device.

III. New 1200V Vertical Structure - LPT

The new 1200V CSTBT chip utilizes an optimized vertical structure based on Mitsubishi's Light Punch-Through (LPT) technology. A schematic comparison of conventional NPT, Epitaxial PT, and LPT chips is shown in Fig. 4. The key to the LPT structure is an optimized n- drift region that it is thin enough to provide low $V_{CE(SAT)}$ while maintaining a robust switching SOA. An n buffer layer is utilized to secure a sufficiently high breakdown voltage and low leakage current in the presence of the optimally thin n- drift region. The thickness of the n- drift layer is selected so that the depletion region extends to the collector when rated voltage is applied in the off-state. However, at normal operating voltages the depletion region does not reach the buffer layer giving an operation characteristic similar to conventional NPT designs. Another feature of the LPT structure is optimized n+ buffer and p collector layers that provide controlled carrier concentration in the n- region during conduction. The result is efficient switching characteristics without the need for carrier lifetime control processing. The new CSTBT chips are fabricated from low cost n-type single crystal (non-epitaxial) wafer material.

IV. New 1200V Low E_{OFF} CSTBT Chip

In the design of an IGBT chip it is possible to trade $V_{CE(SAT)}$ for lower switching losses by adjusting the minority carrier lifetime. Fig. 5. shows the trade-off curve of saturation voltage versus turn-off switching losses obtained for the 5TH generation LPT-CSTBT chip. For high frequency industrial applications a target operating frequency of 40kHz to 50kHz was assumed. Based on this loss simulations were applied to various points along the trade-off curve of Fig. 5 to determine the point of lowest total loss. The optimum point was determined to be around a $V_{CE(SAT)}$ of 3.8V and an E_{off} of 0.028mJ/pulse•A. The carrier lifetime of the 1200V 5th generation CSTBT chip was then adjusted using a new proprietary life time killing process. The resulting chip is optimized for a significantly reduced turn-off switching energy with special attention to losses associated with the tail current because they have been identified as a significant contributor to losses in both hard and soft switched applications. Fig. 6 shows example switching waveforms comparing the new high speed CSTBT to a standard IGBT module. These waveforms clearly show the dramatic reduction in turn-off losses and almost complete elimination of the "tail" current. Fig. 7 shows a comparison of power loss under the condition of 50kHz inductive load chopper operation. The new optimized IGBT provides about a 60 % reduction in total power loss compared to the conventional IGBT.

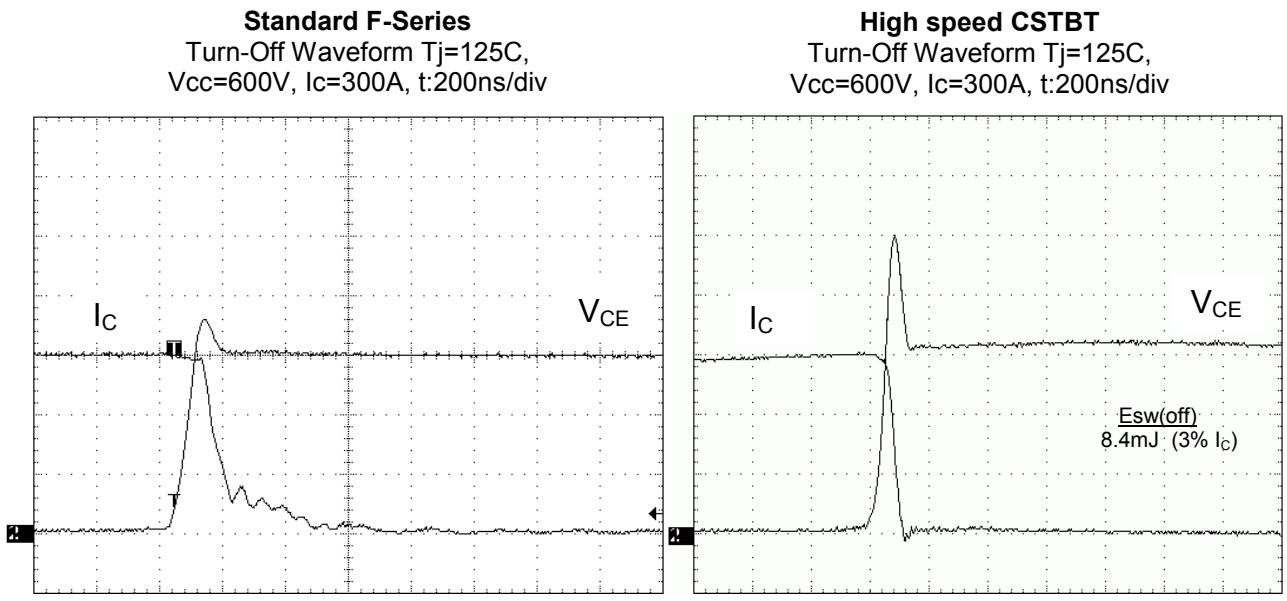

Fig. 6 Turn-Off Switching Waveform Comparison

V. MODULE PACKAGE DEVELOPMENT

For evaluation purposes 300A, 1200V high frequency modules were assembled using a low inductance dual module package. To obtain maximum performance the new high frequency CSTBT chips were coupled with specially optimized free-wheel diode chips having improved fast but soft recovery characteristics and low recovery loss (E_{rr}). The new IGBT module utilizes "U-Package" technology developed by Powerex/Mitsubishi in 1996 [15]. Fig. 8 shows

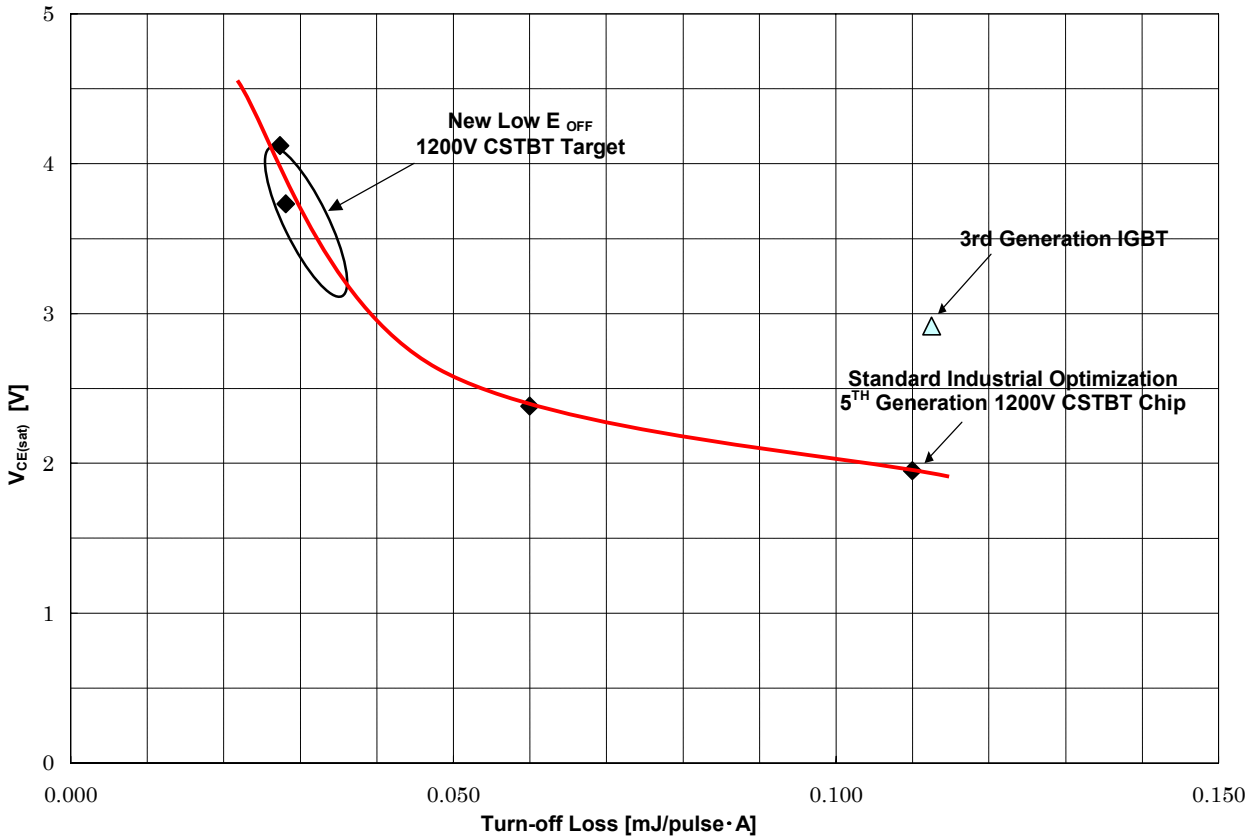

Fig. 5 E_{SW} versus $V_{CE(SAT)}$ Trade-Off for New High Frequency CSTBT

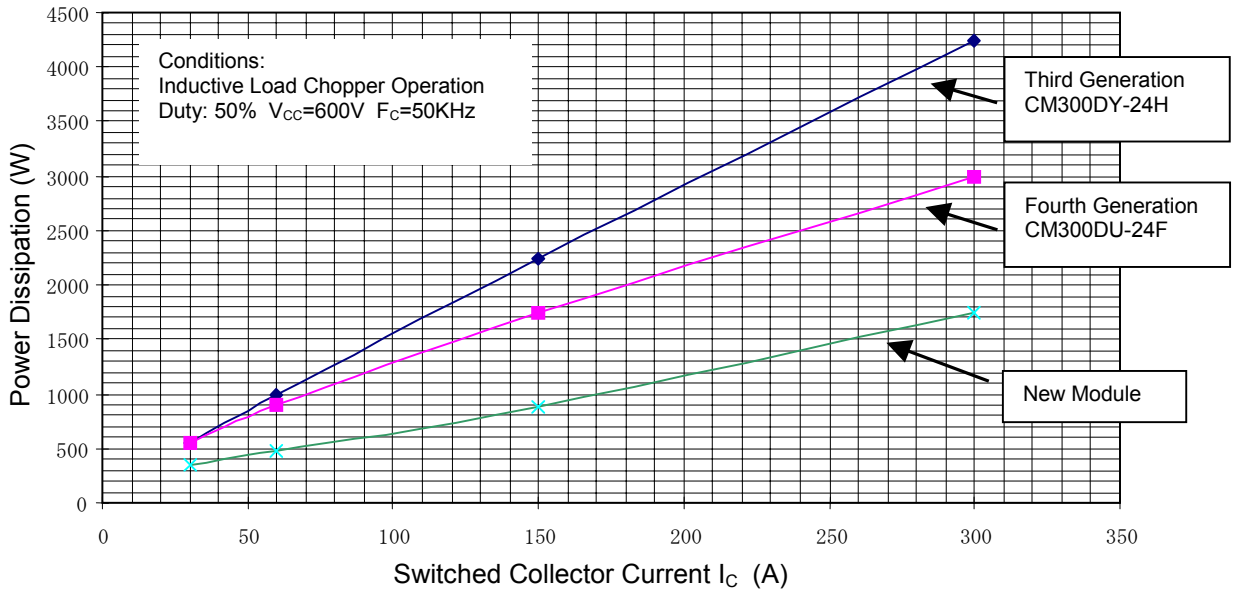

Fig. 7 Inductive Load Hard Switching Loss Comparison

a cross section drawing of the new package. The key innovation is its insert molded case in which the power electrodes are molded into the sides as opposed to inserted after the case is molded. The main electrodes are then connected directly to the power chips using large diameter aluminum bonding wires rather than solder. A photograph of the dual (half bridge) module is shown in Fig. 9.

One of the main objectives in the design of the new package was a reduction in internal inductance. The most significant improvement was made possible by molding wide electrodes into the sides of the case to form parallel plate structures having considerably less inductance than conventional electrodes. In addition, the strain relieving "S" bends that were needed in the electrodes of conventional modules are not needed in the U-Series package because the aluminum bond wires perform the strain relieving function. Elimination of these "S" bends helped to further reduce the electrode inductance. Overall, as a result of these inductance reducing features, the new package has about one third the inductance of conventional modules.

Another advantage of the new package is a significant improvement in manufacturability. The number of soldering steps required is reduced from two to one. With the conventional module, the chip to substrate and substrate to base plate soldering is done first with high temperature solder. Then, the case is attached to the base plate and a second low temperature soldering step is used to connect the power electrodes. In the new module, the second step is eliminated because the connections to the power electrodes are made using the aluminum bond wires. The soldering temperature of the chip and substrate attachment can be reduced helping to minimize the effects of the mismatched coefficients of expansion between the base plate and the AlN DBC substrate. The result is a reduction in thermal stress during manufacturing, improved baseplate flatness, and increased power cycle reliability.

Another advantage of the new package is a substantially smaller ceramic substrate. The ceramic area needed for soldering the power electrodes in the conventional module is not required. As a result, higher performance AlN ceramic

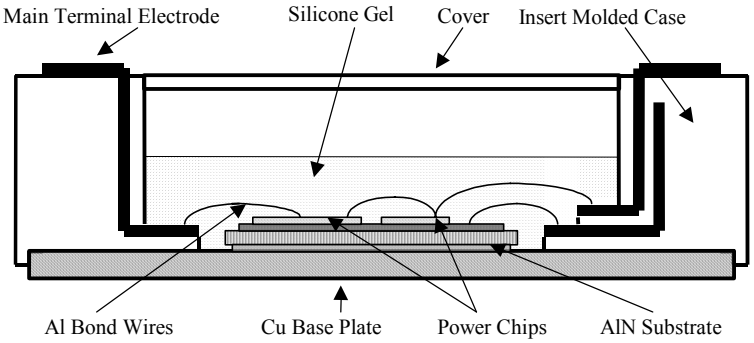

Fig. 8 Cross Section of Low Inductance (U-Package) Module

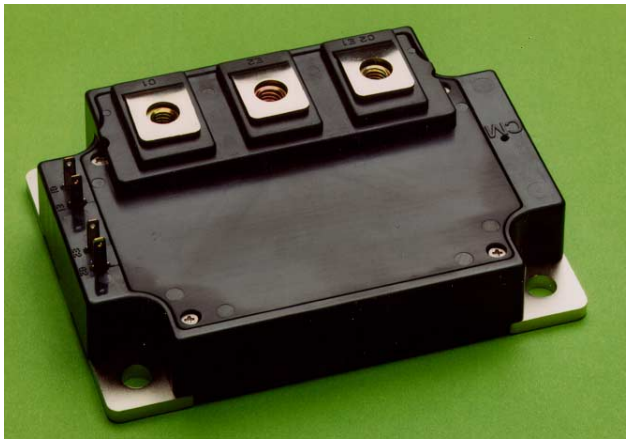

Fig. 9 300A, 1200V Dual (Half Bridge) High Frequency Module

can be cost effectively utilized to minimize the thermal impedance of the new package.

The waveforms in Fig. 6 and loss simulation in Fig. 7 clearly demonstrate the desirable performance of the new module for high power, high frequency applications.

VI. CONCLUSION

A new 1200V high frequency optimized CSTBT module has been presented. The module features an optimized 5TH generation CSTBT chip with less than one third the turn-off loses of the conventional industrial module. The new CSTBT chips are packaged along with optimized free wheeling diodes in low inductance dual packages. The end result is a module package that provides high performance and simplified design in a variety of high frequency industrial inverter applications.

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